

Infineon Successfully Produced First 65nm Samples in Multiple Fabs

Infineon Technologies AG has produced first sample chips in its advanced 65nm low-power and high-performance CMOS platform technology. Infineon leveraged the results of the industry leading 65nm/45nm alliance composed of IBM, Chartered, Infineon, and Samsung (ICIS).

The wafer production was done in the frame of the manufacturing partnership with Chartered. As an early mover to the 65nm low-power version within the ICIS alliance Infineon demonstrates 65nm readiness to all advanced logic programs and offers turn key solutions to all customers facing power-sensitive applications. Infineon's silicon-proven implementations of 65nm MCU-/DSP-cores, libraries, and RF as also analog/mixed-signal macros outperform the crucial performance-to-power ratio known in previous technology generations.

"The data available today emphasizes the multifold strengths of our alliance strategy resulting into a leading position towards time-to-market, figure-of-merits, and manufacturing flexibility by pooling significant R&D resources as also exploiting a huge amount of intellectual capital," said Prof Dr Hermann Eul, Member of the Infineon Management Board and head of the Infineon Communication Solutions Business Group.

For example an ARM9 based subsystem, a major component of mobile phones, a wide spectrum of digital cell libraries as well as a broad variety of SRAM, ROM, RF and analog/mixed-signal functions were verified successfully. The functionality of the ARM9 CPU Core, a DSP as well as all other macro and library elements were proven with silicon from the ICIS alliance in East-Fishkill as well as from the target manufacturing partner Chartered. A first mobile communication product using the 65nm technology has been taped out recently resulting into samples within the first quarter of 2006, the volume production is intended to start in the fourth quarter of 2006.

Infineon defines its cost-competitive Smart Technology Access by offering a turn key solution to its customers, including application-optimized technology flavors, a design system infrastructure open to include customer or 3rd party IP, silicon-proven RF, analog/mixed-signal, SRAM and ROM macros, application tuned libraries, design and silicon prototype services up to volume production capability with its manufacturing partner Chartered.

"Infineon decided to pursue a fast migration into 65nm technology given the optimum trade-off between manufacturing cost triggered by mature 193nm lithography and design-to-cost efficient material innovations in 65nm low-power technology on the one hand. On the other hand this technology reflects a very attractive performance-to-power ratio including best-fit RF parameters", said Hermann Eul. "The 65nm technology will be the technology foundation for the coming years within the Infineon Communication products segment, pushing Infineon's leading position in Baseband and RF CMOS single-chip-integration further ahead of competition and generating additionally volume proposition suitable for all kind of microcontroller and ASIC-based solutions as well."

Source: Infineon

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