Sematech Reveals Details on Practical High-K Metal Gate Systems for 45nm And Beyond

Building on their successful CMOS solution for gate‑first, thermally stable, high-k dual metal gates, SEMATECH researchers have released further data that portends a new era in which future transistor scaling is dominated by heterogeneous integration of new materials onto silicon.

During recent industry meetings, technologists from the world’s leading chip consortium indicated that novel, functional materials systems on silicon, combined with innovative, stable processing technologies, will allow the industry to aggressively increase system-level performance gains.

The new data, available in detail to member companies only, follows SEMATECH’s announcement in January of high-k/metal gate stacks that were used to build high‑performance nMOS and pMOS transistors in a CMOS configuration.

“The scalability of CMOS gate dielectrics, which had been stalled for six years, has been infused with new life by the introduction of manufacturable, performance‑boosting, non-silicon based materials,” said Raj Jammy, director of Front End Processes for SEMATECH.

“These high-k metal systems are practical and mature enough for the industry to use in volume manufacturing with conventional technologies,” Jammy added. “The roadblocks to high-k metal gates have been cleared, and gate stack scaling can move forward again.”

In a series of papers at the recent 2007 Symposia on VLSI Technology and Circuits in Kyoto, Japan, SEMATECH technologists revealed successful identification of candidate systems for nMOS and pMOS metal gate electrodes, along with novel ways to modulate transistor workfunction.

“We have systematically screened various n and p-metal candidates and studied their effects on the dielectric and interface stack,” said Byoung-Hun Lee, manager of SEMATECH’s Advanced Gate Stack Program and a VLSI panelist. “This has allowed us to understand the mechanism that controls the effective workfunction and the final threshold voltage for highly scaled devices. As a result, we’ve been able to identify practical, low threshold voltage and low EOT solutions for CMOS scaling.”

Progress reported in SEMATECH’s VLSI papers included:

-- Ternary metal–aluminum-nitride (M-Al-N) materials suitable for pMOS metal gate electrodes with low threshold voltage, utilizing the gate-first processing approach that is most favorable to current factory capabilities. (Ternary metals include tantalum, titanium, molybdenum, and tungsten.). The resulting chips are likely to enhance the capabilities of cell phones and other consumer products requiring low standby power. The paper reporting these results, “Gate First Metal-Aluminum-Nitride PMOS Electrodes for 32nm Low Standby Power Applications,” was presented by lead author H.C. Wen, a former SEMATECH assignee who has returned to Texas Instruments.

-- A dual-channel scheme using standard activitation annealing temperature to achieve a manufacturable low-threshold voltage (Vt) PMOS device, with a metal electrode/high-k dielectric stack combined with a silicon-germanium (SiGe) channel. The paper on this topic outlined a solution for building a band-edge, high‑k PMOS metal gate with low threshold voltage. The paper, “Band-Engineered Low PMOS VT with High-K/Metal Gates Featured in a Dual Channel CMOS Integration Scheme,” was presented by lead

author H. Rusty Harris, FEP project manager.

-- A breakthrough technique for using an electric dipole to modulate the important workfunction characteristic of a negative-channel field-effect transistor (nFET). This effect is achieved by incorporating various dopants into a hafnium silicon oxynitride (HfSiON) gate dielectric. That composition provides the ability to vary the strength of the dipole, resulting in a “control knob” for workfunction. FEP Project Manager and lead author Paul Kirsch presented the topical paper, “Dipole Moment Model Explaining nFET Vt Tuning Utilizing La, Sc, Er, and Sr Doped HfSiON Dielectrics.”

At SEMICON West in mid-July, Jammy predicted that gate stack solutions from SEMATECH and others will be widely used at the 32 nm technology generation, after introduction at 45 nm by leading-edge manufacturers. However, he said front‑end engineers will continue to face the challenges of integrating new materials for functionality – including such targets as leakage reduction, mobility enhancement, reliability improvement, and resistance reduction.

“If you look at the gate as the brain of the transistor, then changing any of its components is like brain surgery,” Jammy explained. “Change one material, and all the others are affected. Somehow, we need to integrate these novel materials so that they work well together and retain desirable characteristics.”

According to Jammy, successful materials integration is allowing engineers to move beyond using nitrided silicon dioxide (SiO2) as a gate dielectric. This historic material finally reached its limit after successive scaling reduced the thickness of the SiO2 gate dielectric from 90 atomic layers in 1985 to approximately four layers today.

The resulting problems of high current leakage and degraded mobility and reliability have stymied further scaling of gate dielectrics since 2001, Jammy said. Engineers succeeded in circumventing this limitation for three technology generations with strain engineering – but that workaround alone is insufficient for continued scaling in accordance with Moore’s Law.

Successful integration of new gate systems will herald a different future that opens up exciting possibilities and challenges, Jammy continued.

“CMOS and memory scaling will be dominated by what types of materials we harness, and how we process them onto silicon, while continued emphasis will be placed on system-level performance improvement,” he said. Heterogeneous integration on silicon will augment future chips with unprecedented combinations of multigate devices, spin-based devices, molecular electronics, optoelectonic devices, and optical modulators, waveguides and detectors.

Additional emphasis needs to be placed on overall power reduction as well, Jammy added. “What used to be components of leading edge technology are rapidly finding their way into follow-on low-power technologies. Of course, all of this needs to be done with affordable methodologies, without deviating from current manufacturing practices.”

Jammy concluded: “The road to high-k gate stacks is finally clear, and we’re looking ahead to cruise into the materials-driven future.”

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