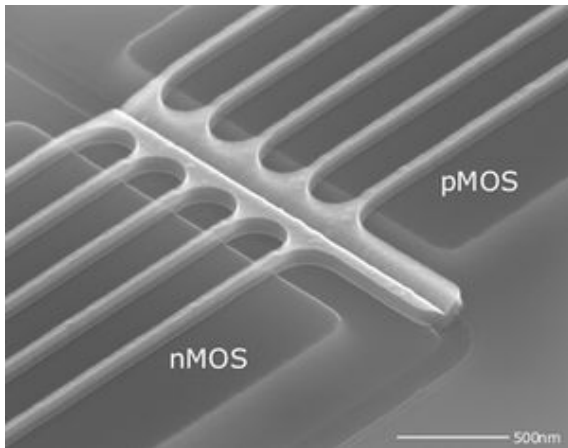


IMEC increases performance of high-k metal gate planar CMOS and FinFETs



Ring oscillator realized with hafnium-based high-k dielectrics and tantalum-carbide metal gates targeting the 32nm CMOS node. Credit: IMEC

At today's IEEE International Electron Devices Meeting, IMEC reports significant progress in improving the performance of planar CMOS using hafnium-based high-k dielectrics and tantalum-carbide metal gates targeting the 32nm CMOS node.

Low threshold voltage (V_t) is achieved by applying a thin dielectric cap between the gate dielectric and metal gate. In addition, the use of laser-only annealing for gate stack engineering resulted in a significant reduction of the minimum sustainable gate length and improved short-channel effect control. The same processes were applied on FinFETs and resulted in a possible candidate technology for the 22nm node.

A major challenge in using high-k dielectrics for CMOS devices is the high threshold voltage resulting in low performance. Dual metal gates in combination with dual dielectrics can solve this problem but have the drawback that extra processing steps are required resulting in a higher processing cost. IMEC developed a simpler, lower-cost integration scheme using only one dielectric stack and one metal.

A thin dielectric cap is deposited between the gate dielectric and metal gate which effectively modulates the work function towards the optimal operating zone. Laser anneal instead of spike anneal is applied to reduce the effective oxide thickness. Using laser-only annealing higher activated and shallow junctions could be achieved.

Both a lanthanum- (La_2O_3) and dysprosium-based (Dy_2O_3) capping layer was used for nMOS and an aluminum-based capping layer for pMOS. Symmetric low V_t of $\pm 0.25\text{V}$ were achieved and drive currents of $1035\mu\text{A}/\mu\text{m}$ and $505\mu\text{A}/\mu\text{m}$ for nMOS and pMOS respectively at VDD of 1.1V and I_{off} of $100\text{nA}/\mu\text{m}$. Successful CMOS integration was illustrated by a ring oscillator delay of less than 15ps.

Since thin gate dielectrics suffer from soft breakdown before the specified lifetime and the failure is difficult to forecast, IMEC developed a time-dependent dielectric breakdown model to completely predict the reliability of the devices. The model is based on the statistical analysis of hard breakdown including multiple soft breakdown and wear out. By applying the model on the high-k/metal gate devices, the excellent quality of the gate dielectrics has been demonstrated.

In strong collaboration with NXP and TSMC, excellent performance (drive current of $950\mu\text{A}/\mu\text{m}$ and I_{off} of $50\text{nA}/\mu\text{m}$ at VDD of 1V for nMOS FinFETs) and short channel effect control were achieved for tall, narrow FinFETs without mobility enhancement. Physical vapor deposition (PVD) and atomic layer deposition (ALD) were compared as metal deposition technique. Since PVD metals are denser and less

porous, PVD of titanium nitride (TiN) electrodes on hafnium oxide (HfO₂) dielectrics gave improved nMOS performance compared to ALD TiN. IMEC also applied the dysprosium-based (Dy₂O₃) capping process on FinFETs resulting in a possible candidate technology for the 22nm node.

These results were obtained in collaboration with IMEC's (sub-)32nm CMOS core partners including Infineon, Qimonda, Intel, Micron, NXP, Panasonic, Samsung, STMicroelectronics, Texas Instruments and TSMC, and IMEC's key CMOS partners including Elpida and Hynix.

Source: IMEC

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