

UMC Expands X Architecture Support - First Pure-Play Foundry to Provide Qualified 90-nm Design Rules

Foundry Fabrication Now Available for Fabless Customers Designing 90-nm X Architecture Chips

The X Initiative and UMC, a world leading semiconductor foundry, today announced that UMC is the first pure-play foundry to release qualified design rules for X Architecture-based chip designs at the 90-nanometer process node. UMC is now ready to accept X Architecture designs from fabless semiconductor companies and its integrated device manufacturers (IDM) partners for fabrication at the 90-nanometer process node.

The X Architecture represents a new way of orienting a chip's microscopic interconnect wires with the pervasive use of diagonal routes, in addition to traditional right-angle "Manhattan" routing. By enabling designs with significantly less wirelength and fewer vias, or connectors between wiring layers, the X Architecture can provide significant improvements in chip performance, cost and power consumption.

"UMC continues to demonstrate its leadership by supporting the X Architecture and its use of diagonal wiring to gain performance and cost advantages," said Patrick T. Lin, chief SoC architect at UMC.

"Through our most recent effort, fabless semiconductor companies can develop 90-nanometer chips that incorporate diagonal routing with the confidence that UMC will support their designs throughout the design and manufacturing cycle."

In 2003, UMC became the first pure-play foundry to join the X Initiative, as well as the first to announce its readiness to accept X Architecture based designs for fabrication at 130-nanometer process nodes.

"UMC's announcement of the availability of world-class manufacturing for 90-nanometer X Architecture designs bodes well for this 'year of first X products'," noted Aki Fujimura, X Initiative steering group member and chief technology officer, New Business Incubation, at Cadence Design Systems, Inc. "The performance and cost benefits of the X Architecture, coupled with the advanced 90-nanometer process, are a potent combination for the performance-demanding and cost-conscious fabless market."

About the X Architecture

The X Architecture, the first production-worthy approach to the pervasive use of diagonal interconnect, reduces the total interconnect, or wiring, on a chip by up to 20 percent and via-counts by up to 30 percent, resulting in significant improvements in chip performance, power and cost. For the past 20 years, chip design has been primarily based on the de facto industry standard "Manhattan" architecture, named for its right-angle interconnects resembling a city-street grid. The X Architecture rotates the primary direction of the interconnect in the fourth and fifth metal layers by 45 degrees from a Manhattan architecture. The new architecture maintains compatibility with existing cell libraries, memory cells, compilers and IP cores by preserving the Manhattan geometry of metal layers one through three.

About the X Initiative

The X Initiative, a group of leading companies from throughout the semiconductor industry, is chartered with accelerating the availability and fabrication of the X Architecture, a revolutionary interconnect architecture based on the pervasive use of diagonal routing. The X Initiative's five-year mission is to provide an independent source of education about the X Architecture, to facilitate support and fabrication of

the X Architecture through the semiconductor industry design chain, and to survey usage of the X Architecture to track its adoption. Representing leaders spanning the entire design-to-silicon supply chain, X Initiative members include: Applied Materials, Inc.; ARM; ASML Netherlands B.V.; Cadence Design Systems, Inc.; Canon U.S.A. Inc.; Dai Nippon Printing (DNP); DuPont Photomasks, Inc.; GDA Technologies, Inc.; HPL Technologies, Inc.; Hoya Corporation; IN2FAB Technology Ltd.; Infineon Technologies AG; JEOL, Ltd.; KLA-Tencor Corporation; Leica Microsystems AG; Matsushita Electric Industrial Co., Ltd.; MicroArk Co. Ltd.; Nikon Corporation; NuFlare Technology Inc.; PDF Solutions, Inc.; Photonics, Inc.; Prolific Inc.; RUBICAD Corporation; Sagantec; Sanyo Electric Co., Ltd.; Silicon Logic Engineering, Inc.; SiliconMap, LLC.; Silicon Valley Research Inc.; STMicroelectronics; Sycon Design, Inc.; Tensilica, Inc.; Toppan Printing Co.; Toshiba Corporation; Trecenti Technologies, Inc.; TSMC; UMC; Virage Logic, Inc.; Virtual Silicon Technology, Inc.; Zenasis Technologies, Inc.; and Zygo Corporation. Membership is open to all companies throughout the semiconductor design chain. Materials can be found at <http://www.xinitiative.org>

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