

TSMC Unveils Nexsys 65nm Process Technology Plans

Taiwan Semiconductor Manufacturing Company, unveiled its newest semiconductor manufacturing process today at a Technology Symposium attended by over 400 of the industry's leading IC companies. First wafers are expected in December 2005.

The new 65nm Nexsys Technology for SoC Design allows designers to build logic devices with double the density of the company's industry leading 90nm technology. This massive integration – the equivalent of more than 750 billion transistors on a single 12-inch wafer – enables significant cost savings to market movers across the IC industry.

Benefits of TSMC's new process technology include a standard cell gate density twice that of TSMC's 90nm Nexsys process; a 6T SRAM cell size of less than 0.5 μ m² (half that of its 90nm counterpart); and a 1T memory cell size that is a 65 percent smaller than the 90nm memory cell.

The 65nm Nexsys technology features an aggressive gate oxide thickness to further enhance transistor performance.

From a power and performance perspective, the 65nm Nexsys technology leads the industry with a 50 percent speed gain (TSMC's 65nm General Purpose process versus its 90nm General Purpose process); and a 20 percent standby power reduction. High-speed 65nm versions are expected to lead the industry in power/performance tradeoffs.

In a novel development born of an earlier process collaboration, an electrical fuse technology has been added to facilitate identification and configuration of devices.

"TSMC is already the foundry leader in 0.13-micron-and-below manufacturing technologies, with volumes and revenues that are multiples ahead of our nearest competitors," said Kenneth Kin, senior vice president, worldwide sales and service at TSMC. "The new 65nm Nexsys technology represents yet another leadership point from which the industry can rapidly accelerate the pace of innovation."

In response to customer demand, TSMC's first 65nm Nexsys technology, which will enter first production in December 2005, is optimized for low power. A high-speed version will be available in 2006, followed later in the year by a general-purpose 65nm process. A version employing SOI technology and an ultra-high-speed version will be introduced in 2007. Logic and mixed-signal options are slated for all versions, with embedded memory available in each.

TSMC's first 65nm silicon was a fully functional SRAM that featured more than 100 million transistors and was validated in April 2004. Since then, some customers including Altera Corp. and others, have taped out and received functional prototypes of their own designs, including logic and memory, for initial validation and benchmarking. Engineers at multiple companies are designing to the process, and tapeouts of production devices are expected to reach TSMC in the second half of 2005.

Early design rules and SPICE models for the new technology have been developed. TSMC libraries will be available in the fourth quarter of 2005, and third party library and IP developers are fast at work developing additional offerings. TSMC's 65nm Nexsys process is supported by Reference Flow 5.0 and will receive additional support as future iterations of the industry-leading design flow are developed. Process and design tools available to engineers are outlined in power and leakage management and design for manufacturing (DFM) guidelines.

The new technology features a minimum number of process changes, such as strained silicon and a new nickel silicide, to shorten time to volume. The 65nm Nexsys technology is the third-generation TSMC process to employ low-k dielectrics and the fourth generation to use copper interconnects.

The 65nm process may be the first-generation process to use immersion lithography techniques, developed in partnership between TSMC and ASM Lithography. A leading proponent of immersion techniques, TSMC took delivery of the first production-worthy 193nm immersion lithography system in 2004. Capable of 132nm wavelengths, the 193nm immersion system also provides a greater than 200 percent depth-of-field improvement versus dry lithography systems. The new 65nm process will be implemented in TSMC's industry-leading 300mm manufacturing facilities, Fab 12 and Fab 14.

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