

UMC Fabricates Record-Setting Voltage-Controlled Oscillator Using CMOS Technology

Chip designed by the University of Florida achieves 105-GHz Operating Frequency

UMC, a world leading semiconductor foundry, today announced it has fabricated a Voltage-Controlled Oscillator (VCO) with a record-setting fundamental operating frequency of 105-GHz using its 0.13um RFCMOS process technology. The chip was developed by the Silicon Microwave Integrated Circuits and Systems Research Group (SIMICS), Department of Electrical and Computer Engineering at the University of Florida, Gainesville.

Until now, the highest recorded fundamental operating frequency for CMOS circuits was a 103-GHz oscillator fabricated using a 90nm CMOS process that consumed approximately four times more power. The new effort by the University resulted in the 105-GHz VCO as well as a second 99-GHz VCO with a tuning range of 2.4 GHz, using the 0.13um process. This effort signifies that VCOs for the 94-GHz industrial scientific medical band and imaging as well as 60-GHz WLAN and 77-GHz radar applications can be implemented using UMC's process. VCOs are used in virtually all RF and wireless systems.

"UMC continues to provide the advanced process technologies that are used to power today's highest-performance applications," said Patrick T. Lin, chief system architect at UMC. "Compared to other technologies used in producing these types of circuits, CMOS delivers the best combination of high performance with low power and low cost for high-volume applications. This latest achievement with the University of Florida demonstrates in working silicon that our RFCMOS process technology is readily able to support very high frequency designs."

"Developing ICs of this caliber in 0.13um CMOS is a huge milestone," said Professor Kenneth O from the University of Florida. "If we incorporate frequency doubling techniques, we should be able to generate signals with frequencies of 200 GHz and higher. This has the potential to open up far-infrared to CMOS. UMC's role in our development was pivotal as this leading foundry provided the process and parameters that brought the chip to silicon quickly and easily."

About the 105-GHz and 99-GHz VCOs

The 105-GHz VCO utilizes a cross-coupled NMOS transistor core. The transistor structure of the LC resonator-based VCO chip has been optimized to reduce parasitic capacitances, which limits the maximum operating frequency. An accumulation mode MOS varactor has been optimized to achieve Q values of approximately 6 at 105 GHz or approximately 630 at 1 GHz, which is critical for achieving low power consumption and reducing noise. The 99-GHz VCO core consumes 15 mW. The phase noise at 10-MHz offset from the carrier varies between -101 to -103 dBc/Hz over the 2.4-GHz tuning range. The circuits were developed with the support of Darpa and announced at the 2005 VLSI Symposium on Circuits in a paper authored by Chang-Hua Cao, Ph.D candidate at the University, and Kenneth O.

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