

UMC Develops Ultimate Spacer Process to Enhance MOSFET Device Performance for 65nm and Beyond

UMC today announced that its Central Research and Development Division (CRD) has successfully developed an Ultimate Spacer Process (USP) technology that simultaneously enhances NMOS and PMOS device performance. Devices fabricated at UMC using USP exhibited drive current improvements of 15% for NMOS and 7% for PMOS, while maintaining overall process simplicity. This accomplishment is instrumental in achieving performance improvement during increasingly difficult CMOS scaling situations.

"Seeking ways to enhance electron and hole mobility is a major focus for device development at UMC," said Dr. Mike Ma, deputy division director of Exploratory Technology for the Central Research and Development division at UMC. "The USP technology enables UMC to provide an extra performance improvement option to complement our other mobility enhancement technologies. With only one additional process step inserted, USP also delivers a manufacturability advantage over other strained silicon technologies."

In addition, the performance advantage of USP can be leveraged with other mobility enhancement techniques; combining USP with substrate orientation engineering resulted in a 35% PMOS drive current enhancement. This USP technology has also been successfully deployed in a customer FPGA product, resulting in a 15% speed improvement without compromising yield and reliability performance. This confirms the readiness of applying USP technology for 65nm mass production and beyond.

UMC will present a detailed report of this technology at the "2005 IEEE International Electron Devices Meeting" in Washington, D.C. on December 7.

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