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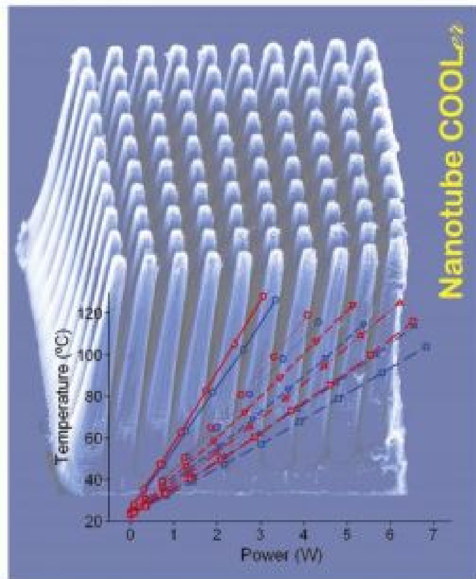
Nanotubes could improve thermal management in electronics



Red graph lines show the temperature of a bare chip as increased power is applied, while blue lines show the reduced temperatures of a chip equipped with a carbon nanotube cooling structure (pictured in the background). Solid and dashed lines represent experimental and computational results, respectively. Both natural and forced convection conditions are noted. Credit: Rensselaer/Robert Vajtai

As the electronics industry continues to churn out smaller and slimmer portable devices, manufacturers have been challenged to find new ways to combat the persistent problem of thermal management. New research published in the March 19 issue of *Applied Physics Letters* suggests that carbon nanotubes may soon be integrated into ever-shrinking cell phones, digital audio players, and personal digital assistants to help ensure the equipment does not overheat, malfunction, or fail.

The chips inside an electronic device give off heat as a byproduct of power consumption when the object is on or being used. To reduce high temperatures, heat sinks – finned devices made of conductive metal such as aluminum or copper – are attached to the back of the chips to "pull" thermal energy away from the microprocessor and transfer it into the surrounding air. Fans or fluids are sometimes used to improve the cooling process, but they increase the device weight, size, and bulk.

Using microfin structures made of aligned multiwalled carbon nanotube arrays mounted to the back of silicon chips, researchers from Rensselaer Polytechnic Institute and the University of Oulu in Finland have proven that nanotubes can dissipate chip heat as effectively as copper – the best known, but most costly, material for thermal management applications. And the nanotubes are more flexible, resilient, and 10 times lighter than any other cooling material available.

"As devices continue to decrease in dimension, there is a growing need for miniature on-chip thermal management applications," said Robert Vajtai, a researcher with the Rensselaer Nanotechnology Center and corresponding author on the paper. "When reduced to sub-millimeter sizes, the integrity of materials typically used for cooling structures breaks down. Silicon becomes very brittle and easily shatters, while metallic structures become bendable and weak."

Carbon nanotubes, however, maintain their impressive combination of high strength, low weight, and excellent conductivity, and the carbon nanotube coolers can be manufactured very cost effectively, Vajtai said.

The researchers have developed a simple and scalable assembly, using an innovative processing and

transfer technique to integrate the nanotube structures on the chip. Thick films consisting of 1.2 millimeter long multi-walled carbon nanotubes were grown and detached from silicon/silicon oxide templates, and a laser was used to carve out freestanding 10x10 fin array blocks. The bottom of the nanotube cooler blocks were then soldered onto the backside of a thermometer test chip that was mounted on a silicon substrate. This technique employs conventional manufacturing methods, providing an easy protocol to transfer and integrate nanotube arrays onto the silicon platforms currently used in electric circuits consisting of miniaturized components, according to the researchers.

Compared to a chip with no cooling source, 11 percent more power was dissipated from the chip mounted with the nanotube cooler. Under forced nitrogen flow, the cooling performance with the fins was improved by 19 percent. "These numbers are consistent with the heat dissipated by the best thermal conductors, and demonstrate the possibility of a lightweight, solid-state add-on structure for an on-chip thermal management scheme which works without involving heavy metal block and fan or fluid-flow procedures for heat removal which can greatly increase the weight of electronic devices," Vajtai said.

The researchers are continuing to explore a variety of techniques to further optimize the nanotube’s cooling capabilities by improving the thermal interface between the chip and the nanotube, enlarging the cooler’s surface area, and perfecting the fin-array geometry.

Source: Rensselaer Polytechnic Institute

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